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ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY MODULE

Inventors: Javesh R. Bhakta et al.

Filed: January 30, 2004 Atty Docket: NETL-001CJ

1 of 9

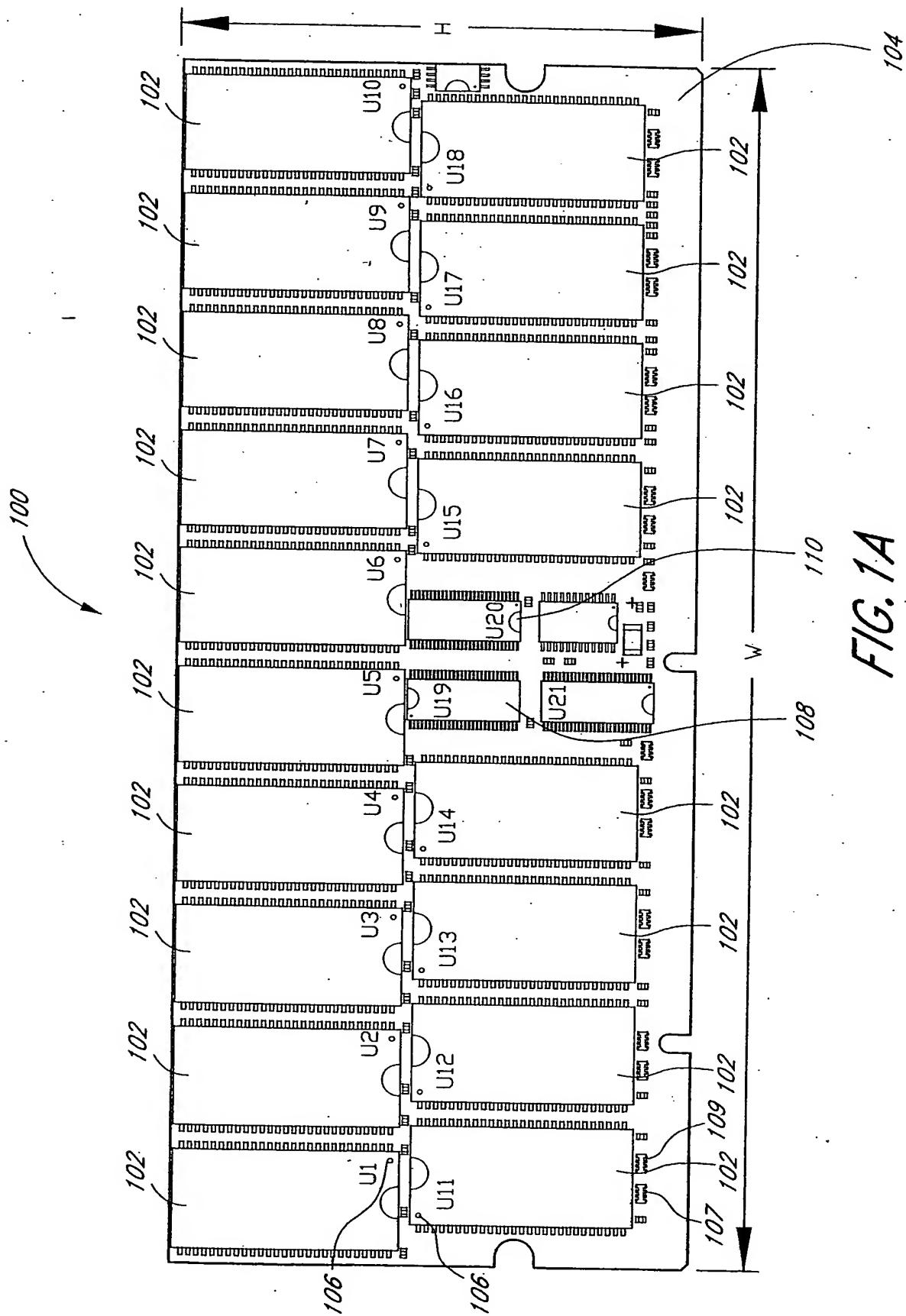


FIG. 1A

ARRANGEMENT OF INTEGRATED CIRCUITS
IN A MEMORY MODULE

Inventors: Jayesh R. Bhakta et al.
Filed: January 30, 2004 Atty Docket: NETL.001C1
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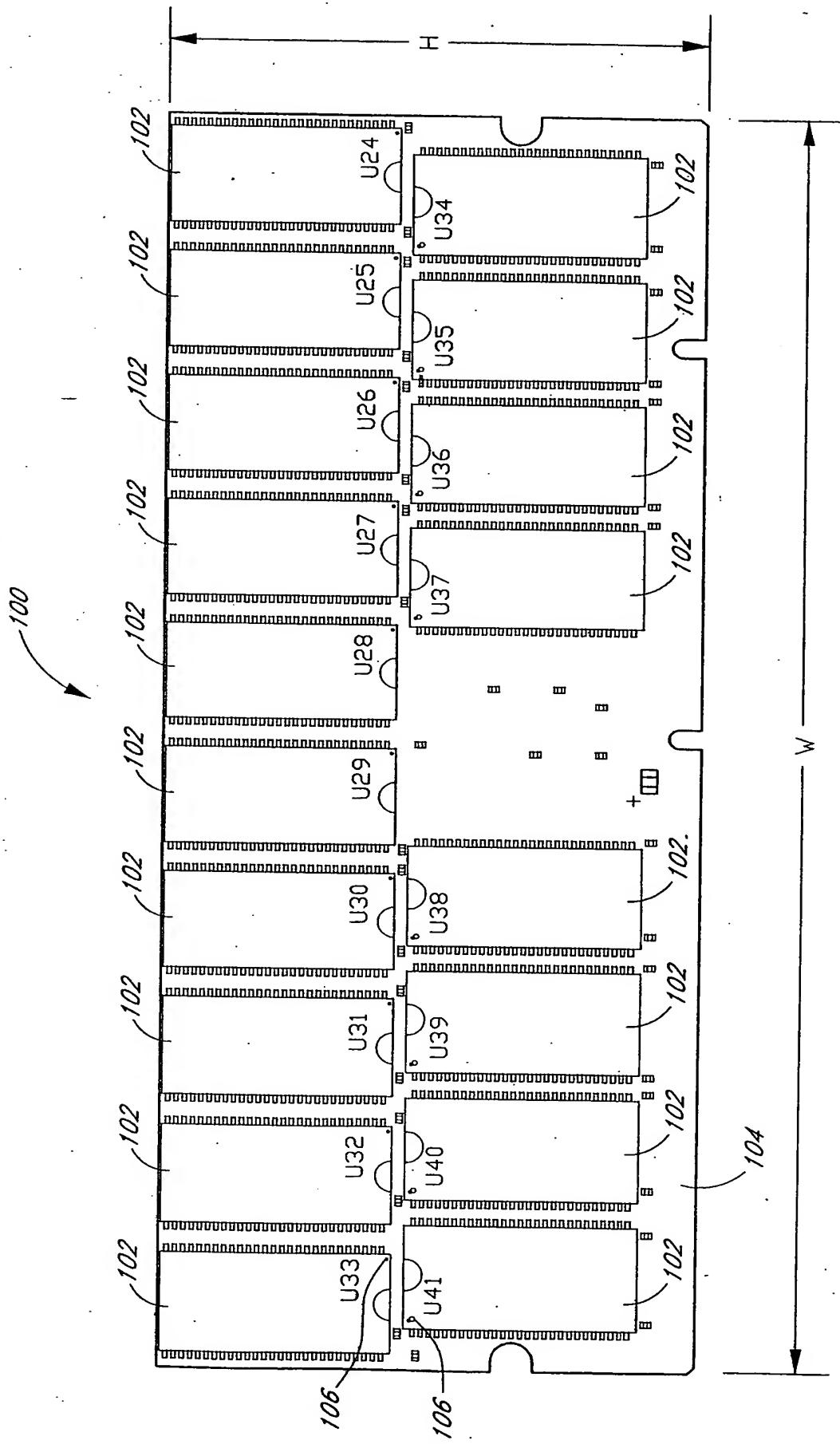


FIG. 1B

ARRANGEMENT OF INTEGRATED CIRCUITS
IN A MEMORY MODULE

Inventors: Jayesh R. Bhakta et al.
Filed: January 30, 2004 Atty Docket: NETL.001C1
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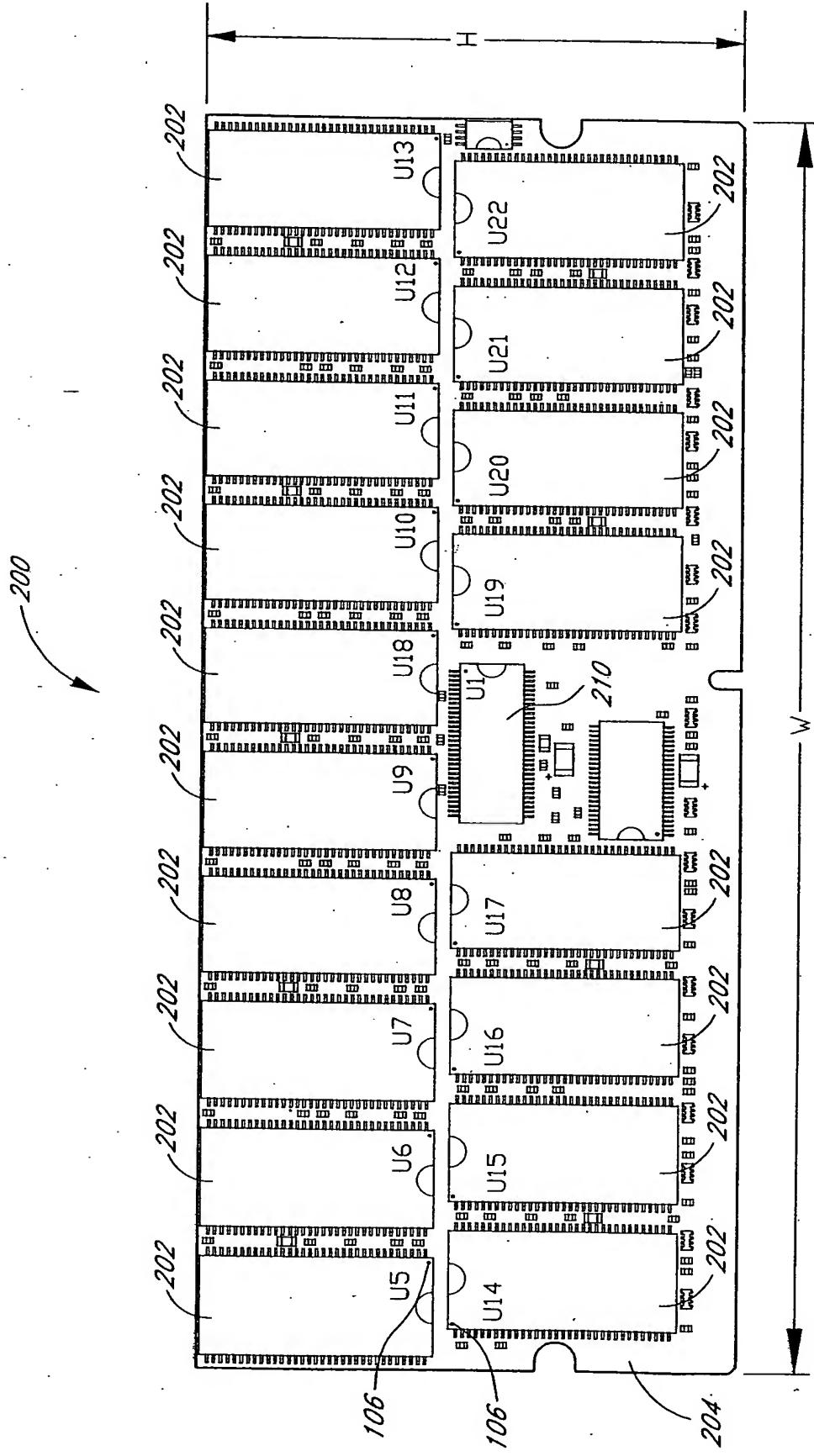


FIG. 2A

ARRANGEMENT OF INTEGRATED CIRCUITS
IN A MEMORY MODULE

Inventors: Jayesh R. Bhakta et al.
Filed: January 30, 2004 Atty Docket: NETL.001C1
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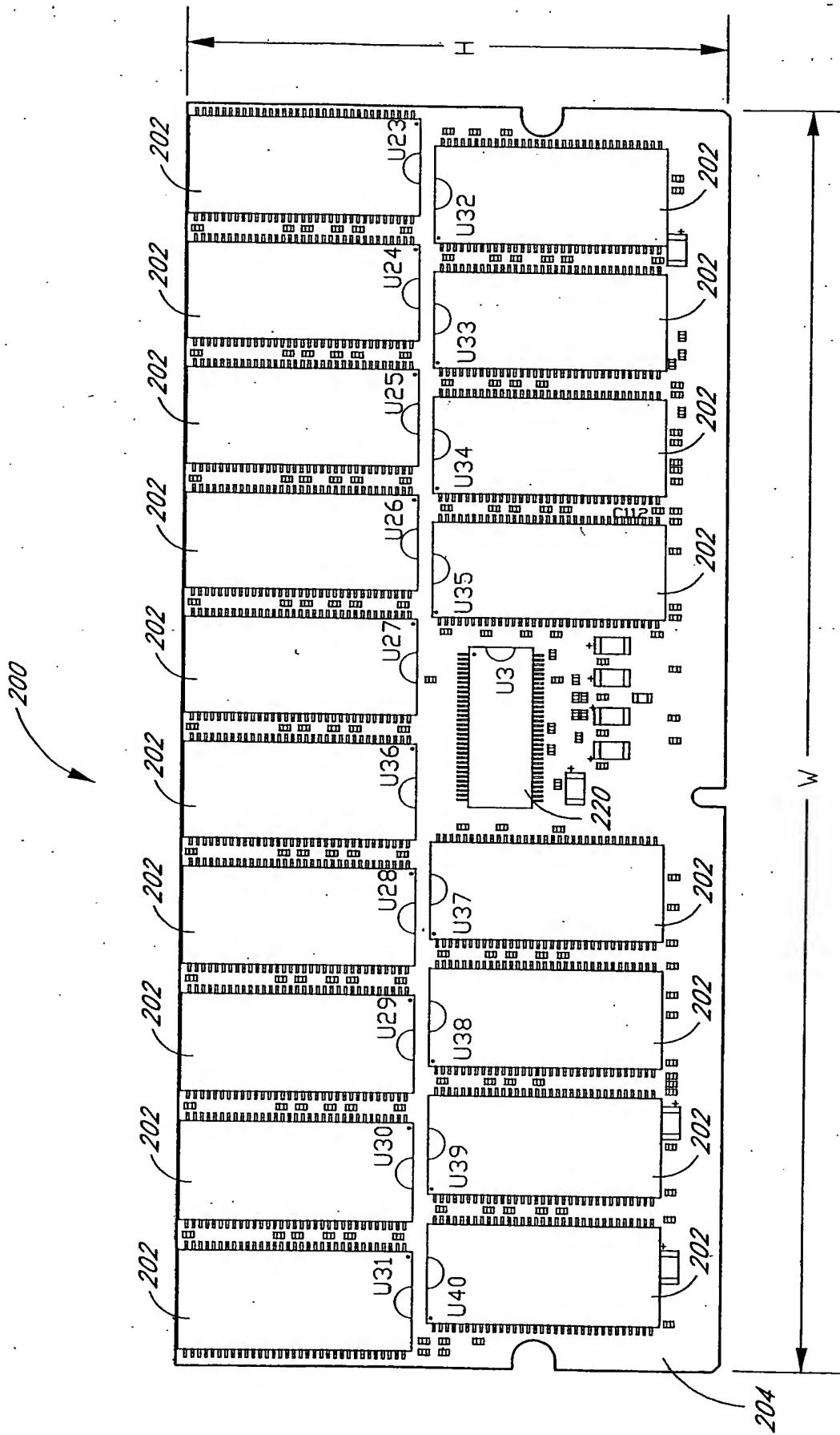


FIG. 2B

ARRANGEMENT OF INTEGRATED CIRCUITS
IN A MEMORY MODULE

Inventors: Jayesh R. Bhakta et al.
Filed: January 30, 2004 Atty Docket: NETL.001CI
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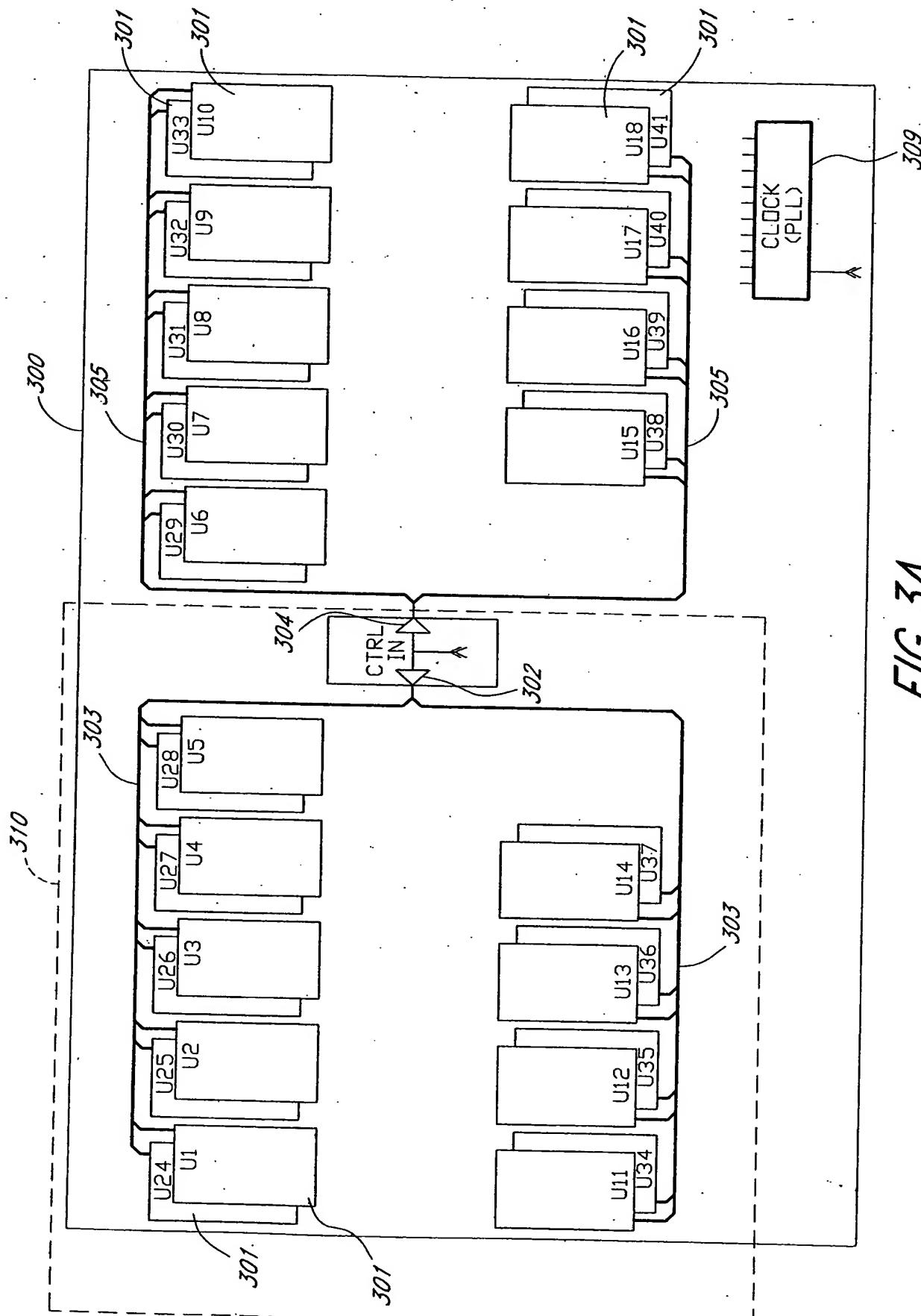
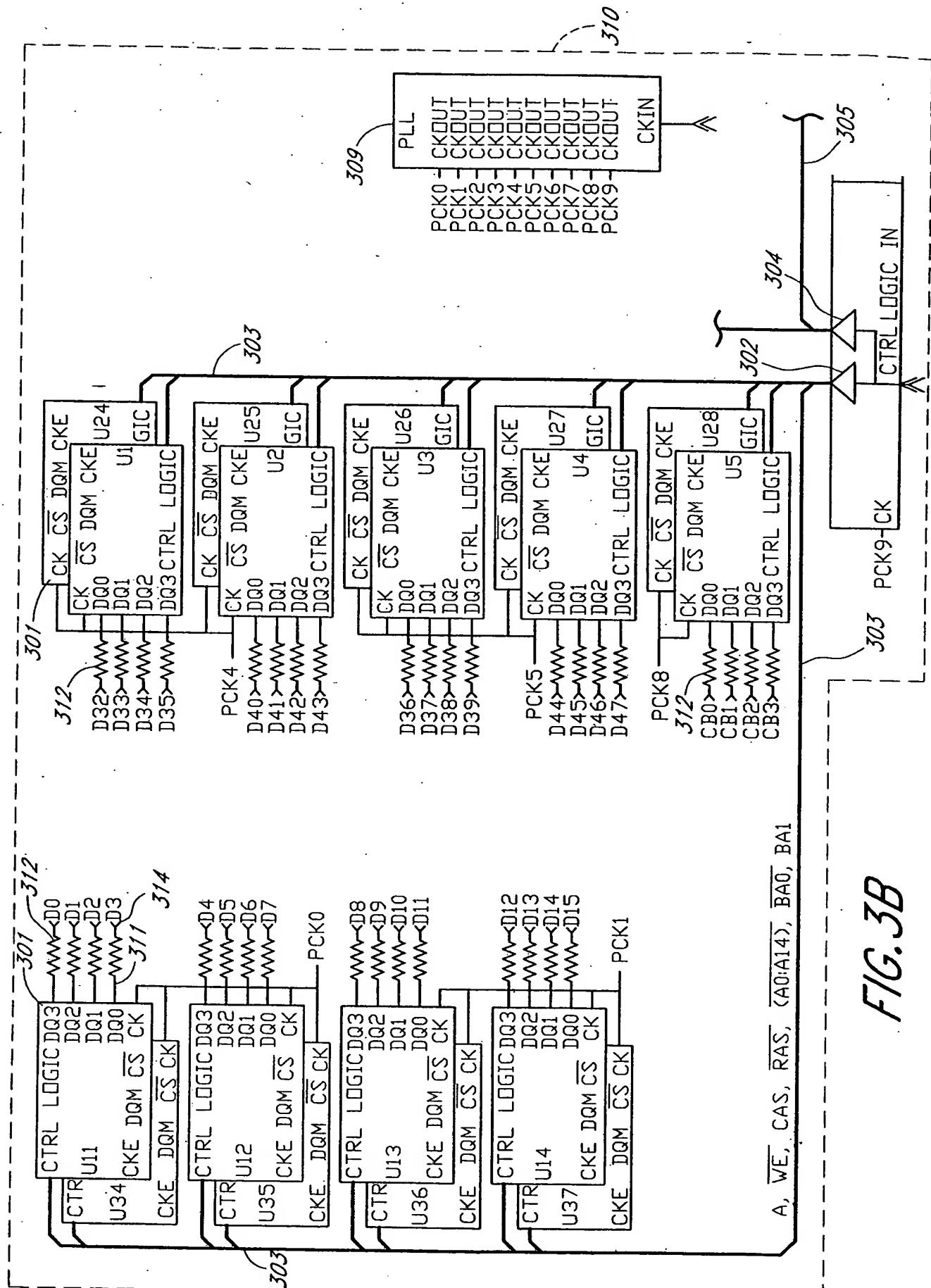


FIG. 3A

ARRANGEMENT OF INTEGRATED CIRCUITS IN A MEMORY MODULE

*Inventors: Jayesh R. Bhakta et al.
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ARRANGEMENT OF INTEGRATED CIRCUITS
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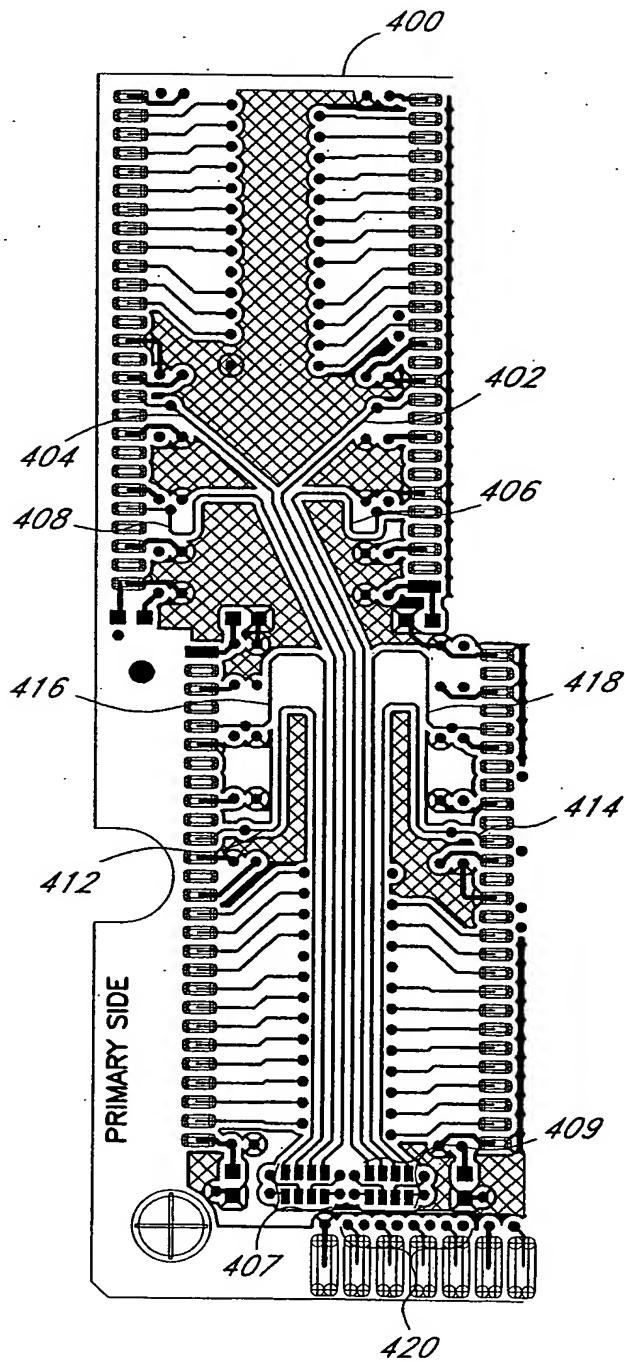


FIG. 4A

ARRANGEMENT OF INTEGRATED CIRCUITS
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Inventors: Jayesh R. Bhakta et al.
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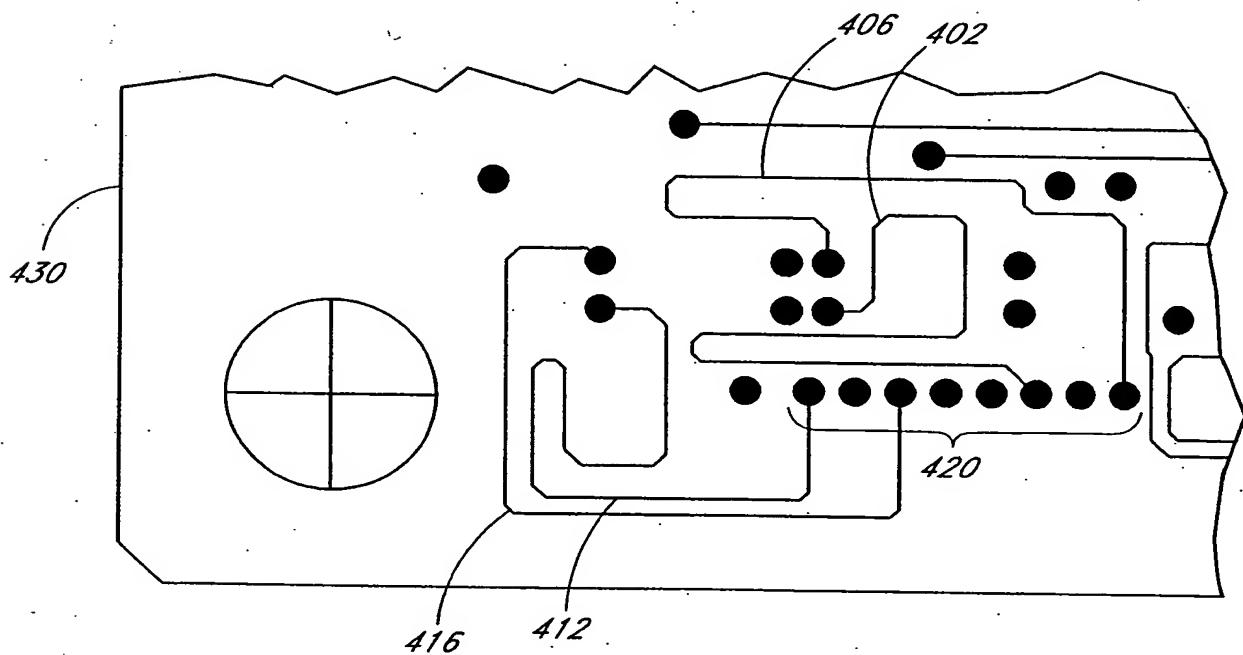


FIG. 4B

ARRANGEMENT OF INTEGRATED CIRCUITS
IN A MEMORY MODULE
Inventors: Jayesh R. Bhakta et al.
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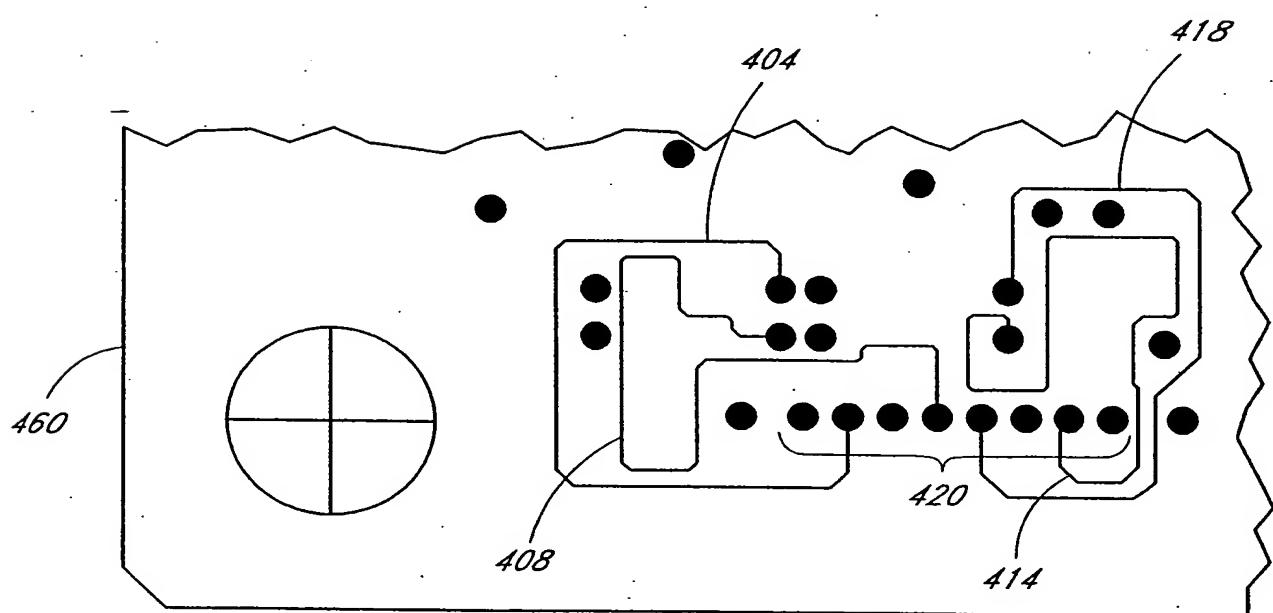


FIG. 4C